

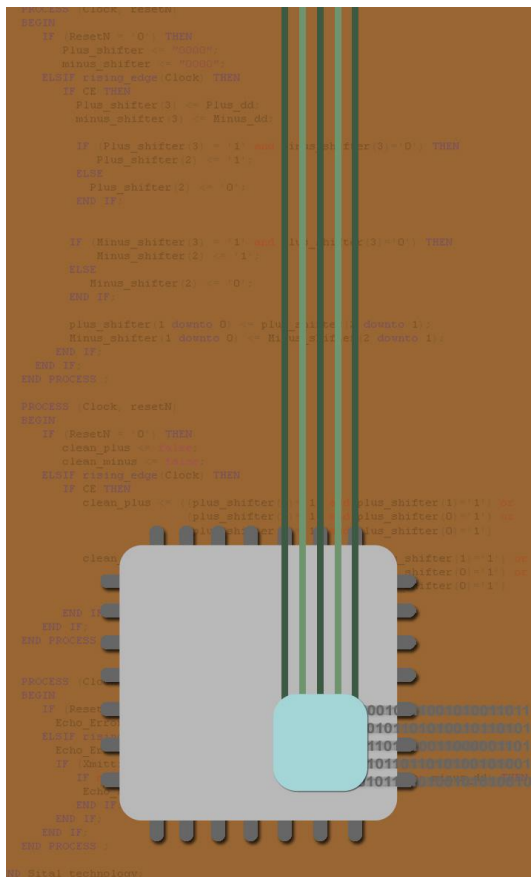
# MIL-STD-1553 IP Core for FPGAs



# RT1553FE

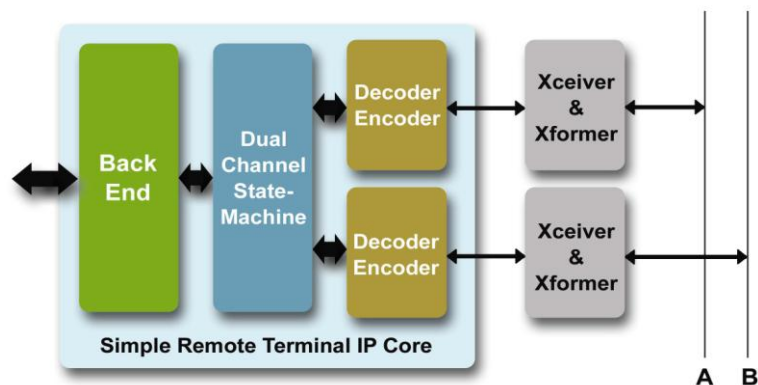
For 1553 Remote Terminal Implementations

Compact, Robust, Reliable  
MIL-STD-IP-Cores



## Key Features and Benefits

- Mil-Std-1553 Intellectual Property for FPGAs and ASIC
- Suitable for any MIL-STD-1553 RT implementation
- Very small FPGA area utilization
- Supports any even clock frequency
- Does not require CPU for management, no SW required
- Modular architecture allowing flexible implementations
- Provided with full verification environment
- Passed full validation testing by 3rd party
- Eliminates risks related to parts obsolescence
- Based on vendor and technology independent VHDL code



Designed from ground up for use in aerospace, avionics and military MIL-STD-1553 solutions, Sital's MIL-STD-1553 IP products, offer uniquely compact, robust and reliable BC, RT, MT solutions for any PLD/FPGA and ASIC device. They were developed following the company's unflagging commitment to quality and excellence along with strict adherence to meeting the stringent requirements of the military and aerospace specifications.

## More IP Cores from Sital:

- MIL-STD-1553 IP Core DDC\* enhanced mini-ACE\* interface
- MIL-STD-1553 Discrete Components Transceiver
- MIL-STD-1553 Obsolete Replacement Services

More information available at [www.sitaltech.com](http://www.sitaltech.com)



## Specifications

### Compatibility

- MIL-STD-1553B Notice 2
- RT Validated according to test plan from MIL-HDBK-1553A
- 1Mbps Data Rate
- Connects to any transceiver-transformer pair

### FPGA Requirements

- 10 pins to connect to transceiver
- Standard FPGA pads

### Clock

- Any even frequency from 12MHz and up

### Supported FPGAs

- Any FPGA with sufficient number of LUTs
- FPGA families from the following vendors:
  - Xilinx
  - Actel
  - Altera
  - Lattice
  - QuickLogic

\* For other FPGAs or ASIC please consult Sital

### RT1553FE Deliverables

- EDIF net list for the core for FPGA family and clock frequency
- User's manual
- Sample VHDL code that incorporates the core
- Synthesis script for sample code

### Available Configurations

- RT1553FE: Remote Terminal only

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## A Core for Simple Implementations

The RT1553FE IP Core is suitable for small and simple Mil-Std-1553 implementations, where no CPU is present or required or where relatively short messages are sent over the bus. The core is particularly useful in space applications, obsolete replacement designs and simple applications.

## Small Gate Count

Sital's MIL-STD-1553 IP requires very small space from FPGA. The following table shows examples of the area usage, in different FPGA devices:

Vendor	Product Family	Area Usage (4-LUT count)
Altera	Stratix, Cyclone	930
Xilinx	Virtex-II, Spartan 3	805
Lattice	LatticeXP	764
QuickLogic	PolarPro	1059
Actel	RTAX-S	1036 Modules

- These numbers are approximate. Other FPGA vendors and families are available
- Actual area usage may vary according to core configuration.

## Backend Interface

The RT1553FE interfaces with the backend through simple address-data read and write "bus cycles".

- No CPU is required
- Simple integration with user's logic

## Manchester Decoder

The unique Manchester decoder can work with any even clock frequency from 12Mhz and up to reduce clock sources and clock domains on board (reduces EMI/RFI). Advanced algorithms for filtering out noise and disturbances enable the core to operate in harsh environments.

## Advanced Verification

To ensure a fully reliable and robust product the core was developed using an advanced verification environment that includes a Random-Generation engine, Code-Coverage and assertion tools. All MIL-STD-1553B functions and performance requirements were verified.

## 3<sup>rd</sup> Party Validation

The RT1553FE IP Core successfully passed the full MIL-STD-1553B Notice 2 RT Validation test, according to a test plan from MIL-HDBK-1553A. Validation tests were performed by an independent 3<sup>rd</sup> party laboratory.

## Simple Integration

In order to simplify the integration of the core, a sample VHDL design that uses the core is provided, including:

- A comprehensive user's manual.
- A VHDL gate level model of the core for the target technology.
- A Transceiver VHDL model that connects the core with 2 buses.
- A bus tester VHDL model that generates 1553 messages and checks the return replies.
- A top Test bench that instantiates all of these components to a working example.
- A simulation script for compiling and running the core.

## About Sital Technology

Founded in 1993, Sital Technology is a leading provider of IP cores and products for Mil-Std-1553.

SITAL Technology's key quality resource is its creative, talented and professional staff. Our engineers are veterans of the Israeli Air Force, who served in the technical units of the F-16 avionics systems. They gained knowledge and experience with the MIL-STD-1553 standard from the bottom up, both as design engineers for MIL-STD-1553 components and as technicians working on the aircrafts.

Among our many customers you can find NASA, Israeli Aircraft Industries (IAI), Rafael, Elbit, Astronautics, Tadiran, Israeli Ministry of Defense, Elta, Honeywell, BAE Systems, RADA and many others.

Represented in USA by:

